

REMARKS

At the outset, Applicants wish to thank the Examiner for the courtesies extended to the Applicants' representative during the telephone interview on January 12, 2011. The remarks presented in this Paper are consistent with discussions with the Examiner during the interview and provide a substance of the interview. The Office Action dated September 2, 2010 has been received and its contents carefully reviewed.

By this Amendment, claims 9 and 30 are amended. Claims 1, 8-9, 11-12, 15-27, and 29-30 are pending in the application, with claims 1 and 8 being identified as withdrawn. Reconsideration and withdrawal of the rejections in view of the above amendments and the following remarks are respectfully requested.

As a preliminary matter, Applicants respectfully request reconsideration of the decision to withdraw claims 1 and 8 from consideration. The outstanding Office Action does not provide any discussions or a decision on the request presented in the Remarks Section of the response filed March 17, 2010. Applicants presented in the March 17, 2010 response that the claim amendments made to claim 1 incorporate subject matter that had been previously recited in dependent claim 3, for which no species or restriction requirements have been made during prosecution, and that there is thus no additional burden on the Examiner to continue to examine claims 1 and 8.

In the Office Action, claims 9, 11-12, 15-27 and 29-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cairns et al. ("Cairns1") (U.S. Publication No. 2002/0030653) in view of Cairns et al. ("Cairns2")(U.S. Patent No. 6,268,841), Enami et al. (U.S. Patent No. 5,892,493), Morita (U.S. Patent No. 6,989,810) and Nitta et al. (U.S. Patent No. 6,661,402). Reconsideration and withdrawal of this rejection are respectfully requested.

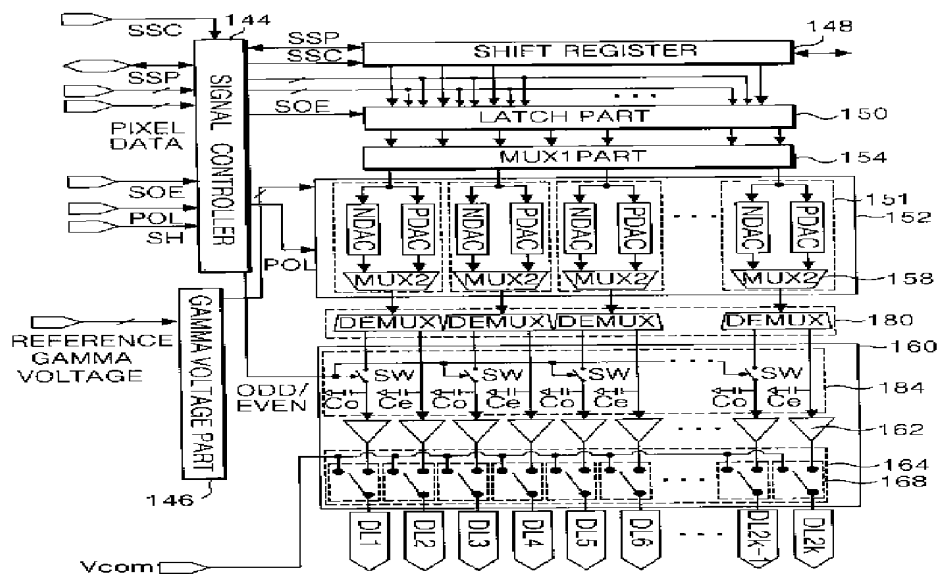
Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "a multiplexer part performing a time-division on the digital pixel data for a plurality of data lines for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; a level shifter part raising a voltage of the

time-divided pixel data directly supplied from the positive and negative paths of the multiplexer part...” None of the cited references teaches or suggests at least these features of claim 9. Accordingly, Applicants respectfully submit that claim 9 and claims 11, 12, 15-27 and 29, which depend from claim 9, are allowable over the cited references.

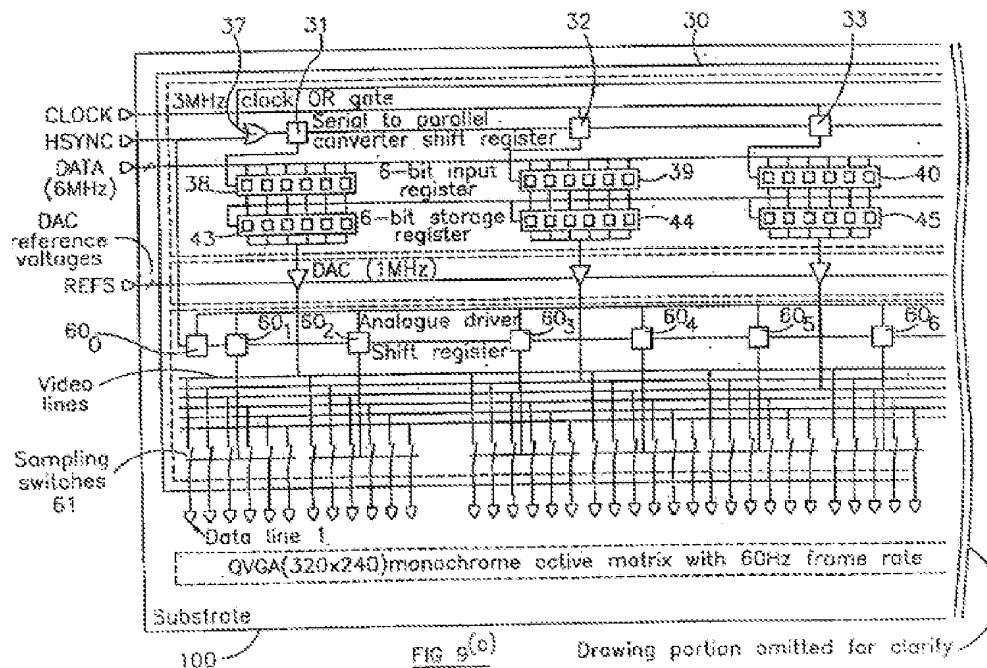
As discussed during the interview, none of the cited references discloses “a level shifter part raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths of the multiplexer part” as recited in claim 9. As recited in claim 9, a level shifter is a separate element different from a shift register. Also, Fig. 5 of Cairns1 merely discloses a pair of MUX and DEMUX used in association with DACs in an effort to reduce the circuit area and the number of transistors. See Cairns1 at paragraph 0015. Cairns1 thus does not disclose “a multiplexer part performing a time-division on the digital pixel data for a plurality of data lines for a first horizontal period using a polarity control signal and an even/odd signal” as recited in claim 9.

In addition, as illustrated in Figure 5, the Vcom voltage in the claimed invention is supplied to the output channels for a disable period of the input source output enable signal of the second horizontal period. Different from the Vcom voltage, Figure 5 also shows the reference gamma voltage supplied to the PDAC and NDAC so as to convert the digital signal to the analog signal.

FIG. 5



At page 6 of the Office Action, the Examiner cites paragraph [0061] of Cairns1 as teaching the aforementioned features of claim 9. However, Applicant submits Cairns1 fails to disclose the aforementioned features of claim 9. As shown below, Figure 9(b) of Cairns1, Cairns1 does not show that Vcom voltage is supplied to output portion between an m phase analog driver 22 and matrix 1.



With respect to paragraph [0061], Cairns1 discloses that DACs 21 receive the reference voltage from common reference voltage bus. However, the reference voltage of Cairns1 corresponds to the reference gamma voltage in Figure 5 of the present application, which is different from the Vcom voltage of the claimed invention. In other words, the Vcom voltage is a separate element different from the reference gamma voltage as discussed above. Accordingly, Applicants respectfully submit that claim 9 and claims 11, 12, 15-27 and 29, which depend from claim 9, are allowable over the cited references.

Claim 30 is allowable over the cited references in that claim 30 recites a combination of elements including, for example, “performing a time-division on a plurality of digital pixel data for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data; raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths using a level shifter...” For similar reasons discussed with respect to claim 9, none of the cited references teaches or suggests at least these features of claim 30. Accordingly, Applicants respectfully submit that claim 30 is allowable over the cited references.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

Dated: January 28, 2011

Respectfully submitted,

By: /Valerie P. Hayes/
Valerie P. Hayes
Registration No.: 53,005
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorneys for Applicant